Combined On-Line/Off-Line Test Solutions for Digital Filters *

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Abstract

A low-cost on-line test scheme for digital filters, capable of providing an off-line BIST solution, is proposed. The scheme utilizes an invariant of the digital filter in order to detect possible circuit malfunctioning on-line and shares most of this on-line checking hardware with off-line BIST. The analysis performed indicates that 100% fault secureness & 100% fault coverage are possible, if certain design constraints are followed.

1. Introduction

The off-line test problem has become increasingly important during the last decade as more and more hardware is integrated into a single chip. The increase in clock frequencies has pushed the cost of ATEs higher, resulting in higher test costs. Consequently, built-in self-test has been increasingly exploited to trade off ATE cost to the cost of on-chip test hardware. On-line test, on the other hand, is gaining importance as we move to deep-submicron technologies, where the probability of failure is increasing. The overhead for hardware requirements of on-line test is usually higher than that of BIST; the type of hardware utilized for off-line and on-line test are distinct in most applications. In this study, therefore, we investigate a low-cost on-line test solution that can share most of the on-line test hardware with a BIST solution. We focus our experiments on digital filters due to their popularity in most current applications.

In this study, we propose a low-cost on-line test solution for digital filters capable of supporting off-line BIST and reducing the cost of on-line test hardware by trading off latency to fault detection. It is further possible to reduce area overhead by trading off some level of fault secureness at the lower bits of the filter. A discussion of these trade-offs is given in section 4. There exist various alternative techniques, such as duplication, error coding [12], or redundant residue systems [3]. However, none is capable of producing a similarly low-cost, moderate latency solution.

The method proposed in this study utilizes a functional invariance of a digital filter, and is therefore comparable to algorithm-based fault detection [7]. In contrast to algorithm-based techniques which utilize certain relationships between the input and output space at a given time instance, the proposed scheme utilizes an input/output relation, which holds only if a wide time range is considered. Use of such a technique introduces latency to the fault detection process. Such latency is inversely proportional to the magnitude of fault effects, thus ensuring rapid fault security for faults with large magnitudes. Out approach also relies on on-line monitoring of inputs and outputs and is thus comparable to input vector monitoring techniques. Yet previous input vector monitoring techniques have consistently higher latency in fault detection independent of the magnitude of the fault effect. Furthermore, the scheme we propose has appreciably lower area overhead than comparable methods. Such area reduction benefits are accenturated since the hardware utilized for on-line test is similar to that of arithmetic pattern generators and can thus provide the basis of a low-cost on-line/off-line test scheme.

The results of the experiments performed in this study indicate that 100% fault secureness is possible within a reasonable latency with low area overhead if certain design constraints are followed. The method is applied to both high and low-pass filters and is proven to be effective. Furthermore, the hardware added for on-line test is also utilized for a low-cost off-line BIST solution which relies on arithmetic pattern generators and response compactors [10], capable of providing very high fault coverage.

We illustrate in section 2 examples of previously developed off-line and on-line test schemes for DSP and motivate the rationale and the application areas for the proposed scheme. While section 3 outlines the determination of the proposed invariant, section 4 further extends the discussion to include how the invariant is utilized in this study. Section 5 provides results and associated explanatory remarks. Furthermore, concluding remarks and possible extensions of the applicable arenas of the proposed invariant-based approach are provided in section 6.

2. Previous Work & Motivation

Off-line test schemes developed for digital filters outweigh comparable schemes developed for on-line test. Examples of off-line test schemes for digital filters can be

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found in [2, 4, 6]. In [2], a short sequence of functional test patterns is proposed, providing fault coverages in excess of 90%; high functional coverage is proven through analysis and high structural coverage is substantiated through fault simulations. Goodby & Orailoglu in [4] develop built-in self-test techniques capable of 100% fault coverage through RT and gate level optimizations that eliminate redundant and random-pattern resistant faults. In [6], a low-cost, parameterizable BIST solution for digital filters is developed through utilization of arithmetic pattern generators.

The work in the area of on-line test of digital filters is concentrated in three categories: use of redundant residue number systems [3, 9], algorithm-based approaches [7], and use of simplified functionality [1]. Redundant residue number systems such as [3, 9] are only applicable to high performance implementations that already make use of residue number systems. In [1], linear functions are utilized as a checking circuitry for nonlinear functions, reducing the area overhead below the level of duplication. However, the technique is only suitable for nonlinear applications. The algorithm-based approaches such as [7] come closest to the technique proposed in this paper. In [7], *Parseval's theorem* [8] is utilized for the FFT algorithm so as to achieve concurrent detection of faults. A similar approach is also utilized in [7] for QR factorization. However, the proposed technique is applicable only when there exists a time-independent relation between input and output, thus limiting its applicability. A generic approach developed in [5] utilizes the idle clock cycles of the functional units for on-line BIST. A low area and performance overhead is claimed; the proposed method is inapplicable for high performance DSP applications though, as hardware units are typically highly utilized.

Not only are most of the techniques previously developed for on-line test of digital filters limited, but additionally, they either require high area overhead or are solely applicable to high performance filters that utilize a residue number system. The algorithm-based approaches can on the other hand be applied only when a time-independent relation exists between input and output. None of these techniques, furthermore, is capable of supporting an integrated low-cost off-line built-in test solution.

To surpass such limitations, we introduce in this study a low-cost technique capable of providing an integrated off-line test solution and applicable even when no time-independent invariant relation exists. Exploiting a time-dependent relation introduces a detection latency to on-line fault detection that is proportional to the time range of the relation. By tolerating a small inaccuracy, this time range can be reduced. While introducing inaccuracy also results in delays in fault detection, the overall detection latency can still be quite low if fault masking is prevented. The time-dependent relation between inputs and outputs of a filter being employed in this work is examined in detail in the next section.

3 Invariant Determination

The functionality of an FIR filter is defined by the following equation.

$$y[n] = \sum_{k=0}^{M} h_k x[n-k] \tag{1}$$

In this equation, the h_k's constitute the coefficients that govern the output characteristics of the filter. M represents the order of the filter; as M gets larger, the frequency response is improved at the expense of increased implementation cost. Calculation of the frequency response of a filter can be effected by taking the *Fourier* transform of the transfer function. Even though calculation of the frequency response requires complex operations, its value at certain frequencies can be derived easily. We utilize the frequency response of the filter at $w = 0$ ($F(w)|_{w=0}$) in order to take advantage of the associated computational simplicity at that point. The response of a filter at $w = 0$ corresponds to the DC gain of the filter, which is equal to the sum of the filter coefficients ($\sum_{k=0}^{M} h_k$).

In order to be able to utilize the DC gain of the filter, in an on-line test scheme, we start by taking the infinite summation of both sides of equation 1. Then we change the order of summation and eliminate k from $x[n-k]$ since the summation is over an infinite range. We conclude by dividing both sides of the equation by $\sum_{n=-\infty}^{+\infty} x[n]$ to arrive at equation 2, which is another way of expressing the DC gain of a filter.

$$\begin{aligned} \sum_{n=-\infty}^{+\infty} y[n] &= \sum_{n=-\infty}^{+\infty} \sum_{k=0}^{M} h_k x[n-k] \\ \sum_{k=0}^{M} h[k] &= \frac{\sum_{n=-\infty}^{+\infty} y[n]}{\sum_{n=-\infty}^{+\infty} x[n]} \end{aligned} \tag{2}$$

However, for a relation to be applicable in an on-line test environment, it should be determinable from a limited set of input/output values. The same relation derived over a limited time range yields:

$$\sum_{n=0}^{N} y[n] = \sum_{k=0}^{M} h_k \sum_{n=0}^{N} x[n] + Tolerance \tag{3}$$

$$|Tolerance| \leq 2 \sum_{k=1}^{M} k h_k x_{max} \tag{4}$$

where x_{max} denotes the maximum input signal magnitude. $Tolerance$ depends only on filter coefficients and the maximum input magnitude. As can be seen in equation 3, an increase in the number of inputs results in a diminution of the effective impact of tolerance on invariance uncertainty. In the next section, we propose an implementation of an on-line test scheme for digital filters with low cost and reasonable fault detection latency.

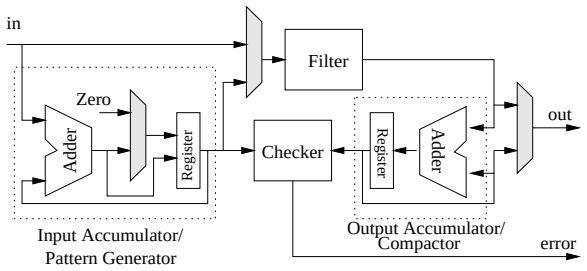

Figure 1. On-line/off-line BIST hardware

4. Method

The proposed method is first applied to a 13-tap low-pass filter, which is implemented in the transposed direct form. A fractional number system of the form 1.11 (1 bit for the sign and 11 bits for the fraction) is chosen for the input. The output is truncated to be in the form of 1.13. The filter coefficients are converted to canonical-signed-digit form and the constant multipliers are implemented as a number of shift-add operations.

The relation derived in the previous section is utilized as in the following form:

$$\left| \sum_{k=0}^{M} h_k \sum_{n=0}^{N} x_n - \sum_{n=0}^{N} y_n \right| \leq Tolerance \qquad (5)$$

As shown in figure 1, an adder and a register is introduced both to the input and output of the circuit in order to calculate $\sum_{n=0}^{N} x_n$ and $\sum_{n=0}^{N} y_n$. The shaded multiplexers in the figure are utilized only if an off-line BIST solution is required. The accumulated input is multiplied with $\sum_{k=0}^{M} h_k$ and the accumulated output is subtracted. The absolute value of the difference is compared subsequently with the off-line computed tolerance. If the result is not within the acceptable range, an error is reported. While equation 5 establishes a sufficient theoretical basis for this technique, its applicability to real-life designs needs to be undertaken through an analysis of its fault detection capabilities. In such an analysis, we need to be sensitive to fault masking effects.

In addition to fault masking effects, a couple of additional points need to be considered in order to expose the efficacy of the method. We start with a discussion of the underlying adders. The effect of a fault at the n^{th} bit position of an adder to the output will be 2^{n-B}, where B is the output width of the filter. The tolerance of the filter used in this study is around 2^3, as determined by equation 4. Therefore, in order for a fault at the n^{th} bit position to be detected, it has to be activated 2^{B+3-n} times; the faults at the sign-bit position will be detected after 8 activations and the faults at the least significant bit will be activated after 2^{17} patterns. Assuming that the least significant bits are activated at a 50% rate, a fault at the least significant bit will require 2^{18} patterns to be detected. This wide divergence in the number of patterns required is correlated with the magnitude of the fault effect. In addition to the positive correlation with fault effect magnitude, the likelihood of fault activation also impacts detection latency. If a fault is unlikely to be activated, it will not be rapidly detected. Transient faults are unlikely to be detected by the proposed scheme unless they are persistent or show fault effects of high magnitude.

The accumulators introduced at the input and output of the filter are required to be larger in width then the input and ouput widths, since they are used to accumulate a long sequence of patterns. The width of these accumulators and the width of the operations in the checker circuit can be reduced if the input spectrum is known to be a zero (or low) mean spectrum. Another way of reducing the bitwidths is by trading off fault secureness at the low order bits. Reducing the bitwidth of the accumulators will shorten the intervals between successive clearing of accumulator registers, which is necessary to prevent overflow. This will in turn eliminate the detection capability of faults at the low order bits since, according to the analysis, such faults are detected with higher latency.

Assertaining fault security levels for an on-line application necessitates knowledge of the input patterns. While a knowledge of the distribution of the input patterns may be usable to provide an analytical understanding of the fault security levels attained, such analysis provide limited results for narrow domains. Assuming no prior knowledge of the input patterns in an on-line environment necessaitate a realiance on fault simulations methods for assertaining fault security levels. We therefore utilize simulation-based techniques with random patterns in order to establish fault security levels of our scheme. The setup in Figure 1 is utilized during fault simulations by assuming that only the *error* output is observable. The *error* output is always precisely $zero$ for a fault-free circuit. Detection of a fault during fault simulations indicates that the fault causes the *error* output to attain the value of one, guaranteeing that the fault will be detected during circuit operation.

Fault simulation, in general, is a computationally complex process. Additionally, in our case, the limited output observability and the sequential loops introduced by the accumulators cause the fault effect to remain in the circuit for a long time prior to its detection and thus increase the complexity of fault simulation. Therefore, a deterministic fault sampling technique is utilized in order to guarantee coverage of faults at each bit position and reduce the complexity of fault simulation. Fault simulations are performed on three adders selected at the leftmost, middle, and rightmost position of the filter taps.

5. Results

Two 13-tap filters, one high-pass and one-low pass, are implemented and fault simulations for the on-line test scheme are performed on both filters. The simulations for off-line test, on the other hand, are only performed on the

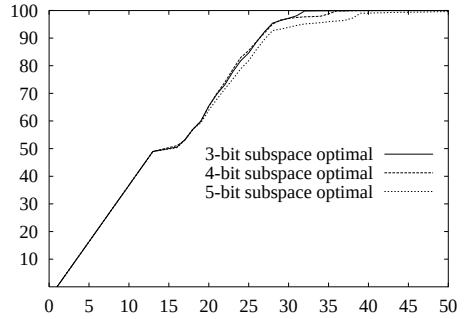

Figure 2. Fault coverages for off-line test

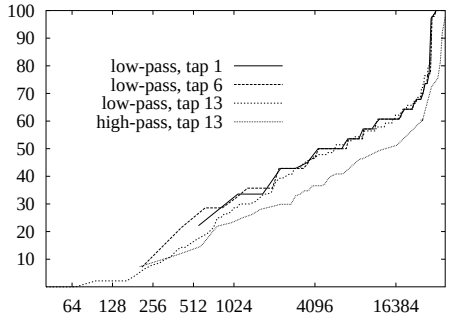

Figure 3. Fault coverage for on-line test

low pass filter. The filters are optimized and mapped in advance to the LSI_10k library by a commercial logic synthesis tool. The hardware added for on-line test is also utilized with the addition of three multiplexers that are shown as shaded in figure 1. A test signal causes the filter inputs to be supplied from an arithmetic pattern generator. The initial seed and increment for the pattern generator are supplied from the circuit inputs possibly with a low speed tester and the patterns generated on-chip are applied at speed. The outputs are compacted at the output accumulator and observed at the output at the end of the off-line test session through the output multiplexer. Even though the on-line test scheme does not introduce any performance overhead to the filter, the additional multiplexers included for off-line test add a small delay to both the input and output of the filter. The fault simulation results for off-line test are presented in figure 2 for three types of arithmetic pattern generators [10]. Even though the fault coverage figures are quite promising for the filters utilized in these experiments, the optimizations proposed in [4] for random-pattern testability of digital filters may need to be performed for larger filters.

Figure 3 shows the results of fault simulation performed on both filters. The results indicate that fault detection increases as expected up to the 80% range. At that point, there is a sudden jump in fault coverage figures. A possible explanation for the jump is that the activation probability of the faults at the low bits is quite high. However, further detailed analysis indicates that an additional reason for this unexpected jump consists of numerical inaccuracies caused by truncation errors. Truncation errors, in addition to helping reduce the latency for the faults at the low order bits, may also cause false alarms. The use of a relative tolerance, while capable of solving the problems caused by truncation errors, forces disabling of on-line error checking for a number of patterns, increasing both fault simulation complexity and fault detection latency. A combination of the two schemes, on the other hand, both improves the fault simulation speed and eliminates possibility of false alarms. In order to further differentiate among high versus low bit faults, analysis of the bit positions of the faults caught at analogous pattern counts needs to be undertaken. We report on this analysis in table 1, which supports the magnitude-based differential latency aspect, outlined in section 4.

The impact of the scheme on performance is negligible since the scheme solely observes the inputs and outputs of the circuit. The area overhead, on the other hand, is considerable, particularly for smaller designs. For example, the area overhead for the experimental benchmarks is around 25%. Nonetheless, for larger filters the same area overhead will constitute an appreciably smaller percentage of the design. The input and output accumulators (constituting 50% of the total overhead) can additionally be utilized as off-line BIST hardware, resulting in 1% extra overhead for the multiplexers introduced to enable off-line test.

Finally, we examine the effects of the faults in order to be able to prove that they are not being masked while being accumulated. We start with an examination of fault effects at the RT level. At this level, with no resource sharing, the linearity of filter structure guarantees that unidirectional fault effects at the block level result in unidirectional output effects. In other words, the RT components are required to have unidirectional fault effects.

For an analysis at lower levels, a gate level implementation needs to be identified. We outline the type of analysis and issues by utilizing ripple-carry adders in this work. A fault at the i^{th} bit full-adder carry output effects the output of the adder by 2^{i+1} while any other full-adder fault effects the output by 2^i. If the fault is a stuck-at-0 fault, then the actual output will never exceed the correct output. Conversely, the fault-free output never exceeds the actual output in the case of a stuck-at-1 fault. The same conclusion is reached upon considering register faults. However, these conclusions are only valid for faults at the inputs and outputs of the full-adders and of the flip-flops. The commercial tool utilized introduces faults only at the inputs and outputs of these cells, since they are defined as primitive cells in the LSI_10k library. Under this fault model, the proposed

	Bit positions in the adder													
Patterns	13	12	11	10	9	8	7	6	5	4	3	2	1	0
128	4	2												
512	4	8	10	4										
1024	8	10	10	10	6	1								
4096	8	10	10	10	10	10	6	1						
16384	8	10	10	10	10	10	10	10	6	1				
Total	8	10	10	10	10	10	10	10	10	10	10	10	10	10

Table 1. Detected fault locations

Inputs	Output	f_{10}	f_{20}	f_{51}	f_{11}	f_{21}	f_{30}	f_{40}	f_{31}	f_{41}
000	0	0	0	1	1	1	0	0	1	1
001	1	1	1	2	2	2	1	0	0	1
010	1	1	0	1	0	1	0	1	1	0
011	2	2	1	2	1	2	3	3	2	2
100	1	0	1	1	1	0	0	1	1	0
101	2	1	2	2	2	1	3	3	2	2
110	2	3	3	3	2	2	2	2	3	3
111	3	2	2	2	3	3	3	2	2	3

Table 2. Full-adder outputs for certain faults

scheme produces 100% fault secureness.

An idealized analysis of the effects of the faults internal to the primitive cells is futher undertaken in this study. A simple-full adder implementation, as illustrated in Figure 4, is utilized for this purpose. Fault simulation is performed in order to record the outputs of this full adder circuit for all possible faults. The simulation results indicate that 9 out of the 26 simulated faults violate the unidirectional fault effect requirement. The simulation results for these faults are reported in table 2. Three of these faults possess unequal numbers of patterns that shift the output in divergent directions. The remaining six have equal number of shifts in either direction; those are identified as "Problem Faults" in figure 4. However, a NAND/NAND implementation of the XOR gates in the depicted full-adder cell reduces the number of faults that violate the unidirectional effect property to three, one of them still being $f_{5@1}$. Further studies examining both the feasibility and cost of alternative adder implementations displaying solely unidirectional fault effects can be undertaken.

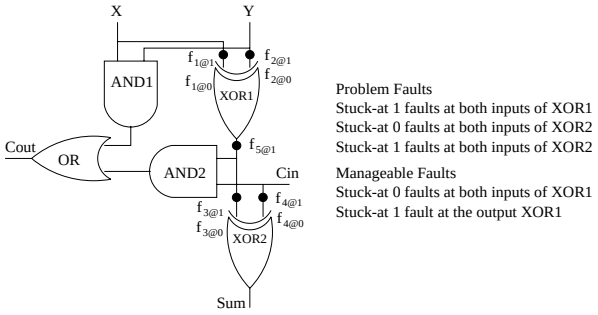

Figure 4. A typical full-adder implementation

6. Conclusion

In this paper, we propose a functional property for on-line digital filter test that is invariant over an infinite time range. When considered within a finite time range for actual on-line execution, the invariance leads to tolerance effects that need to be considered during analysis. Selection of a proper tolerance guarantees that no false alarms exist.

In order to verify the proposed scheme, a test setup is created in order to evaluate the proposed scheme. Intelligent fault sampling schemes are utilized in order to be able to deal with the inordinate time complexity of the problem. Though initial fault simulations indicate very high fault coverages, further analysis of the schemes indicates that fault masking can degrade fault coverage. In order to eliminate the fault masking problem, the primitive components of the circuits need to be modified so as to ensure that the fault effects at the output are unidirectional.

An interesting future extension consists of applying the proposed invariance-based approach to linear pipelined datapaths. In such datapaths, the relation between input and output is time dependent unless a number of successive inputs in excess of the pipeline depth are stored. For these circuits, the time average behavior of the circuit may be investigated as a low-cost on-line test solution. Achieving similarly strong results in such alternative domains may help establish the proposed invariance-based technique as a substitute for existing on-line test techniques, especially for cost-critical applications.

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