An Examination of PRPG Selection Approaches for Large, Industrial Designs

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Abstract

A study for selecting effective PRPGs for large industrial designs is undertaken. For the PRPG selection process, guidance from a set of ISCAS benchmark circuits is initially sought. The set of benchmark circuits used is shown to be ineffective in providing material guidance. The alternative of PRPG selection through actual design experimentation is examined and its weaknesses identified and outlined. A brief DFT analysis is outlined to indicate the importance of early PRPG selection.

1. Introduction

The recent boost in device complexity has increased the intricacy of test generation and application. With the introduction of core-based designs, application of test patterns, once trivial, has become a challenge. Techniques developed for reducing test generation complexity have imposed performance and area overhead in addition to a substantial multiplication of tester memory requirements (primarily for scan based designs), thus pushing up overall manufacturing costs.

Over the past several years, therefore, efforts have been undertaken to reduce manufacturing cost through the utilization of BIST techniques [4, 5, 8, 9]. While reducing the manufacturing test cost, BIST introduces additional area overhead. However, the intrinsic ease of BIST application introduces the possibility of utilization of such techniques in multiple stages of design validation, thus amortizing the inherent area cost across various validation steps.

Typical large industrial designs nowadays consist of over 100k gates and many include a diverse variety of building blocks, such as SRAMs, FIFO structures, random logic and multiple clock domains. We use an industrial design that exhibits such current design attributes as part of our experimental framework. Such design attributes cause a sizable number of hard-to-test faults and an increase in the complexity of the search process for an appropriate PRPG.

The PRPG candidates examined in this study are LFSRs [6], GLFSRs [9], and CA [5]. The lack of results in sequential circuit PRPG selection leads frequently to a random walk search process. The computational requirements of such a search process force us to examine the possibility of guidance from benchmark circuits, such as possibly ISCAS89 [3]. Considering the sheer size of today's large industrial designs, the hypothesis of whether benchmark circuits provide material guidance to PRPG selection is examined initially. Our studies indicate that ISCAS circuits do not provide a clear guidance capability, even though fault simulation experiments substantiate the sizable fault coverage variation that results from the utilization of various PRPG methods.

In this study, such fault coverage variations are identified through fault simulations with various parameters, such as polynomials and seeds. The simulations performed indicate that PRPG selection has a significantly higher effect on fault coverage for no-scan designs than full-scan designs. However, even in the case of no-scan designs, simulations are unable to pinpoint a specific PRPG as the best generator. Barring further research, the results obtained suggest that the selection of the optimal PRPG needs to rely on an analysis of the circuit under test. Consequently, the same search process is undertaken for the aforementioned design. The variable effect of PRPG selection is substantiated further on a large industrial design with significant scan content. While the effect is appreciable, the low base coverages achieved force us to undertake a study of coarse-grain DFT improvements. Results of testability analysis and corresponding DFT recommendations are consequently also presented in this study.

2. Previous Work

Test of large industrial designs requires a considerable amount of DFT hardware. Various testability features need

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to be included in order to test parts of the design that are not accessible under normal circuit functionality. This section presents various techniques developed for improving BIST capabilities of the circuits.

In sequential circuits, a sizable number of faults may remain undetected unless the appropriate initialization is undertaken. Also a single uninitialized bit could corrupt the MISR rendering it useless. In [10], it was shown that most of the circuits can be initialized through pseudo-random patterns. In [8], BIST approaches that rely on test point insertion are shown to be capable of producing up to 100% fault coverage in partial scan designs. C.-J. Lin *et. al.* show how to control the input pins and observe the output pins through boundary scan techniques. Techniques for inserting test points capable of providing increased controllability and observability to areas with hard-to-test faults are outlined in [8].

While researchers have previously examined methods for test improvement through test point insertion, an additional possible research focus is an examination of PRPGs specifically targeted to the designs being considered. These approaches examine issues such as mapping pseudo-random patterns into deterministic ones [2] or reducing the test sequence length by finding proper seeds through discrete logarithms [7]. While such approaches may achieve an improved fault coverage in reduced test time, they also impose some rather difficult limitations to scan-based designs as they necessitate an LFSR of length at least equal to the number of inputs.

In a similar vein, techniques to improve BIST coverage by storing a number of compacted deterministic test patterns as LFSR seeds have been proposed in [6]. However, due to the large number of patterns required for random resistant faults, the additional area cost for storing compacted deterministic patterns may easily outweigh the cost of applying these patterns by testers.

3. Preliminaries

The benchmark circuits utilized in this study include multipliers (s349, s420), traffic light controllers (s298, s400), controllers (s386, s510), and various other industrial designs with unspecified functionality (s9234, s38417). Detailed information about the benchmark circuits can be found in [3].

The industrial design examined in this study has a gate count of approximately 300k. There are 30k sequential elements (10k flip-flops and 20k latches) in the design. Of the 10k flip-flops, approximately 90% are scanned. None of the latches, on the other hand, are scanned. The scanned flip-flops are distributed over 25 scan chains, which are distributed across three clock domains. Three 12-bit PRPGs drive the inputs of the scan chains and the scan chain outputs are observed on three 12-bit MISRs. A simplified version of the BIST configuration and the test environment are shown in Figure 1, which illustrates the limited pin accessibility in the test environment.

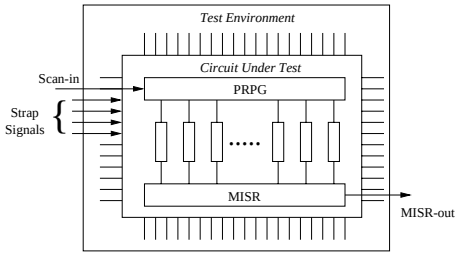

Figure 1. Test environment

The sequential aspects of the design force us to use serial fault simulation, resulting in high computational cost. Consequently, fault sampling techniques are used for fault simulation of the industrial design. The analysis of the effects of fault sampling techniques on fault coverage figures can be found in [1]. In brief, the results of the analysis for the aforementioned industrial design indicate that the error is less then 2.1% for fault simulating a 1% sample (approximately 5000 faults).

While LFSRs are the most commonly used pattern generators for BIST, they suffer from the high number of test patterns required for circuits demanding a wide variety of patterns. Consequently, researchers have been investigating new alternatives for PRPGs, possibly with slightly higher area overhead. CA [5] and GLFSRs [9] have captured the attention of researchers in this area due to their ability to provide increased randomness, thus resulting in possibly reduced test lengths. In this study, therefore, we focus on obtaining approaches for differentiating among LFSR, GLFSR, and CA.

4. Experiments and Results

The experiments are performed on a set of benchmark circuits to seek guidance for an appropriate PRPG to be used with large industrial designs. While the results illustrate the variable effect of PRPG selection, especially in the case of no-scan ISCAS benchmarks, they are unable to illustrate a consistent, distinct superiority in favor of one of the alternatives. Both the challenges undertaken and the associated PRPG-based variations are examined in reference to a large industrial design that constitutes the second part of our experimental framework.

4.1. Fault simulations for ISCAS89 Benchmarks

Fault simulations are performed for a subset of the benchmark circuits with CA, GLFSR, and LFSR. For each generator, three initial seeds and additionally in the case of LFSR and GLFSR, three polynomials are selected. Fault

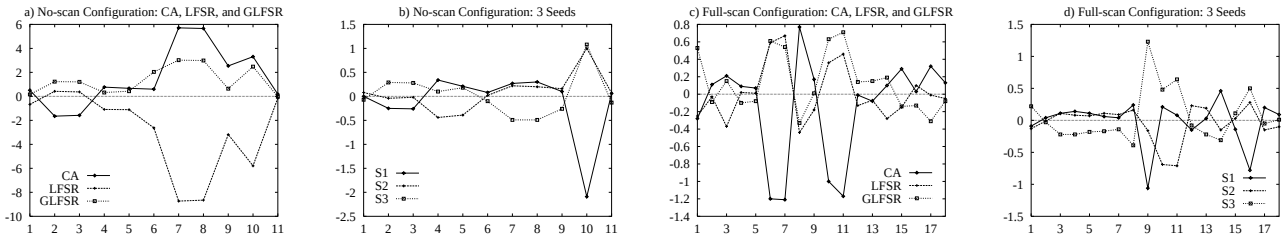

Figure 2. Fault simulation results for benchmark circuits

coverage is captured at pattern lengths of 1k, 2k, 4k and 16k in the case of the no-scan configuration and 512, 1k and 2k pattern lengths in the case of the full-scan configuration. However, the number of patterns is kept limited to 2k for large circuits in the no-scan configuration (indicated by * in Table 1).

To facilitate the presentation of the large number of fault simulation results, we summarize them by taking various averages. Thus, averages across the unweighted space of seeds and polynomials for each PRPG type are obtained for both the no-scan and the full-scan configurations. Averages across the unweighted space of PRPG types and polynomials for each seed examined are also obtained for both configurations. To facilitate a graphic presentation and to emphasize the possible deviations, the overall average across the complete unweighted space of seeds, polynomials, and PRPG types is subtracted from all the previously described averages and used in the graphic presentations in Figures 2-a,b,c, and d. In these figures, the numbers on the horizontal axes correspond to the benchmark circuits in the increased order of the number of interconnect lines (denoted by the number following the letter *s* in benchmark names).

Table 1 identifies a subset of the benchmark circuits simulated in full scan configuration and shows the fault coverage results (averaged over all 84 generators) for 16k test patterns (2k, in the case of starred circuits). The results shown in Figure 2-a indicate that an LFSR is the least effective pattern generator for all but two circuits. Both CA and GLFSR lead in terms of effectiveness in a number of circuits. While the ISCAS benchmark study seems to indicate a clear weakness in the case of LFSRs, no clear superiority between GLFSRs and CA is established. The results summarized in Figure 2-b indicate that no particular seed establishes consistent superiority.

Table 2 identifies a subset of the benchmark circuits simulated in full-scan configuration and shows the fault coverage results for 2k patterns. The results shown in Figures 2-c and 2-d indicate that none of the parameters of polynomial, initial seed, and type of the PRPG, significantly effects fault coverage in the case of full scan designs. This is mostly due to the fact that ISCAS benchmark circuits are easily testable with random patterns in full-scan configuration.

The results indicate that the effect of PRPG selection is not significant in the full-scan case and as in the no-scan case, no particular pattern generator exhibits consistent superiority. Each of the generators has a set of circuits for which it is superior and no associated relation with circuit size is established. Though the results still indicate an overall weakness in the case of an LFSR, it is, nonetheless, the most effective generator for two benchmark circuits.

4.2. Fault simulations for the actual design

As a consequence of experiments performed on benchmark circuits, fault simulations for an appropriate PRPG selection are undertaken for the design outlined.

We undertake our study of PRPG selection by initially converting the embedded PRPG structures into a type-2 LFSR. Results of applying PRPG patterns up to 1000 captures are shown in Figure 3-a. In this figure, the horizontal axis shows the number of captures and the vertical axis shows the associated fault coverage levels. The knee of the curve can be observed to be around 500 captures and the maximum attainable fault coverage with the current LFSR configuration can be inferred to be around 71%.

We also run fault simulations for 100 captures starting from various initial seeds. For the randomly selected polynomials, a length of 100 captures was preferred due to the high computational requirements of fault simulations. Sim-

Name	Coverage	Name	Coverage	Name	Coverage
s344	95.17	s1196	88.42	s1494	54.70
s349	94.71	s1238	84.02	s15850.1	23.85*
s820	41.72	s1423	44.99	s35932	72.44*
s832	40.74	s1488	55.52	s38584	16.92*

Table 1. Average fault coverage: no-scan

Name	Coverage	Name	Coverage	Name	Coverage
s420.1	77.57	s832	91.06	s9234	76.25
s510	99.89	838.1	58.74	s13207	82.05
s526	97.68	s953	92.85	s13207.1	82.91
s641	97.13	s1238	87.35	s15850	88.00
s713	91.15	s1488	99.16	s38417	88.28
s820	92.77	s1494	98.44		

Table 2. Average fault coverage: full-scan

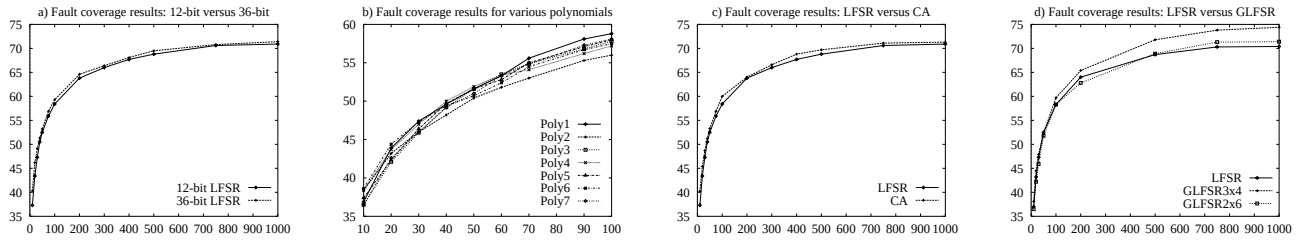

Figure 3. Fault simulation results for the design examined

ulations show that neither polynomial nor seed choice significantly effects fault coverage. Figure 3-b shows fault coverage versus captures for some selected polynomials. The results thus attained exhibit close agreement with the results of the original polynomial. We therefore argue that for this class of designs, a search neither of the polynomial nor of the initial seed space significantly increases fault coverage.

As the linear dependencies embedded in 12-bit LFSRs may be responsible for the reduced fault coverage, we modify the three 12-bit PRPG structures embedded in the design through the appropriate interconnect modifications so as to instantiate a 36-bit LFSR. Simulation results shown in Figure 3-a indicate that the 36-bit LFSR does not exhibit superiority over the 12-bit LFSR.

The PRPG structure is further modified in order to generate interconnect structures necessary for a 12-bit additive CA [5]. The CA fault simulation results are shown in Figure 3-c and exhibit close agreement with the results of LFSR. The high levels of correlation are due to the high number of test patterns involved. Even though the identical number of test patterns is utilized, the slight variations in fault coverage are due to pattern order, which impacts fault coverage because of sequential design aspects.

Finally, two 12-bit GLFSR structures (in (2,6) and (3,4) configuration) are generated to be examined. Figure 3-d summarizes the results of the simulation performed with these GLFSR structures. While the (2,6) configuration does not provide significant improvement over LFSRs, the (3,4) configuration provides 3-4% higher fault coverage than either of the two pattern generators previously examined. This statistically significant improvement in the case of GLFSR (3,4) at somewhat low levels of overall fault coverage necessitates a look at the impact of coarse grain design-for-test improvements.

5. Testability Analysis & Corresponding DFT Recommendations

The previous set of results, be it in the case of ISCAS circuits or in the case of an industrial design, illustrate the ensuing variability due to PRPG selection and the associated need for early PRPG selection guidance. By introducing an examination of the coarse-grain design-for-test improvements, in the case of a large industrial design, we wanted primarily to emphasize the fundamental economic underpinnings of test decisions by bringing into sharp focus the underlying tradeoff between PRPG selection and design-for-test; obviously, if judicious PRPG selection can deliver fault coverages, otherwise to be attained through costly DFT, improved PRPG selection methodologies and design flows need to be sufficiently examined. But furthermore by concentrating on coarse-grain DFT improvements, largely impervious to PRPG selection, we show the preservation of the significant variability in fault coverage results at the high-end of the fault coverage spectrum.

Testability analysis is accomplished by decomposing the fault coverage information down the design hierarchy levels and thus comparing the results of various pattern generators at lower module levels.

Analysis of fault simulations shows that certain parts of the design are completely untestable, while significant parts of the design show major testability problems. Comparing the detailed results of the LFSR and GLFSR simulation, we observe that there is no clear pattern as to the superiority of either PRPG form at the unit level. However, for some units, fault coverage is quite low regardless of the pattern generator.

One of the untestable units is the *cunit* (a performance observer sub-block), which does not have any scanned flip-flops in it, thus possibly causing controllability and observability problems. Scan insertion is possible with little area and almost no performance overhead. However, thorough analysis shows that the *cunit* has only observability problems. The outputs of this unit feed solely IO pins. Consequently, including boundary scan in the design should solve

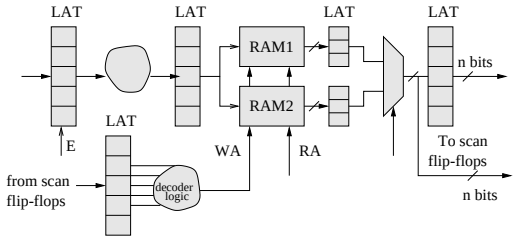

Figure 4. SRAM structure

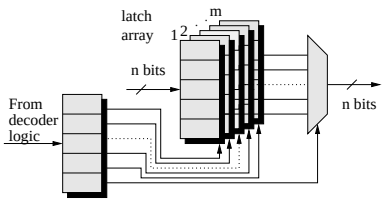

Figure 5. FIFO structure

the testability problems of the *cunit* at the same cost as inserting scan into the *cunit*.

Another block with low coverage, shown in Figure 4, contains built-in SRAM blocks. In the simulations, SRAMs have not been initialized to a known state, resulting in very poor fault coverage. Including dedicated BIST hardware for SRAMs will increase the fault coverage by 3%, which is the size of the SRAM block. While initialization of the SRAM was tried, it did not improve the testability of the units fed by SRAMs since the outputs of the SRAM drive the scanned flip-flops only. On the other hand, significant impact on the decoder logic at the output of the SRAM blocks was observed when the SRAMs are initialized.

A general source of fault coverage loss stems from the FIFO queues utilized in certain blocks. Figure 5 shows the general structure of one of the FIFO queues implemented in the design. FIFO queues constitute about 5% of the design. Slight design-for-test modifications to the FIFO buffer structures, such as test capabilities for circular buffer configuration, may significantly improve fault coverage. A circular buffer structure is preferable over FIFO buffers because pushing data into all the buffers in a circular structure is a much easier task.

Combining the results of fault simulations and analyses for major testability problems, we observe that it is possible to increase the fault coverage level to over 85% by following the recommendations outlined in this section. However, increasing fault coverage beyond this level is expected to require the assistance of fine-grained approaches such as test point insertion.

6. Conclusion

In this study, methodologies for effective PRPG selection are examined thoroughly. Initially, the hypothesis of whether benchmark circuits (ISCAS89, in this case) provide material guidance to PRPG selection is examined. The results indicate that for full-scan designs the high levels of fault coverage attained obscure the possible variation in fault coverage due to PRPG selection. The material variations due to PRPG selection become increasingly evident during an examination of the no-scan variants of the ISCAS89 benchmarks. While the variation is evident, no clear guidelines emerge as to the superiority of a particular PRPG type. While the hypothesis of eventually developing sets of benchmark circuits, capable of differentiating among various PRPG aspects, cannot at his point be discounted, the only industrially meaningful approach at this point seems to be reliance on fault simulations on the actual design.

In more detail, the experiments performed in this study reveal that neither the length of the LFSR nor the polynomial significantly effects the fault coverage. The type of the PRPG, on the other hand, could significantly effect the fault coverage. However, the search for the optimal PRPG suffers from insufficiencies of currently available tools. We observe that the quality of fault sampling and the inefficiency of fault simulation are the main deficiencies of the tools. Use of tools with improved fault simulation and sampling techniques can be expected to improve the effectiveness of the search process.

Acknowledgments

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